ATM SWITCHING SYSTEM AND METHOD FOR SWITCHOVER BETWEEN WORKING CHANNEL AND PROTECTION CHANNEL IN AN ATM NETWORK

FIELD OF THE INVENTION

The present invention relates to a method for switching over between working channels and protection channels provided in an ATM (asynchronous transfer mode) switching system and equipment in an ATM network.

BACKGROUND OF THE INVENTION

To improve network reliability against failures, the following means have conventionally been applied in an ATM network, where a protection channel is provided in addition to a working channel.

(1) Automatic protection switching (APS) of the physical layer (hereafter referred to as the 'physical layer APS') which is defined in SDH, SONET and the like, or

(2) Path re-establishment and switchover using signaling procedure.

The above methods, however, have disadvantages shown below:

In the method (1), a bandwidth for a protection channel must constantly be reserved corresponding to bandwidth of a physical channel. This reduces efficient use of network resources. In the above method (2), long interruption time against normal service is needed because of substantial time consumption for exchanging signals between nodes, and for executing a software process sequence to search for an idle route and to carry out

path establishment and switchover.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method and equipment for switchover between a working channel and a protection channel in an ATM network, with a simplified and efficient manner to compensate the aforementioned disadvantage of the physical layer APS.

A method and equipment for addressing the above issue of the present invention to switch over between a working channel and a protection channel in an ATM network includes the following steps: indicating in a cell for transmission whether the cell is object for channel switchover; duplicating the cell in each connection; transmitting the duplicated cell simultaneously both to a working channel and to a protection channel; and selecting a received cell according to an indication whether the cell belongs to a connection currently in working state.

Preferably, a cell not indicated as being in a connection currently in working state is discarded.

Furthermore, preferably, the indication of cell of which connection is not object for the switchover is specified at the unit of a connection group.

Other features of the present invention will be apparent by the following description on the embodiments of the invention referring to the accompanied drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a basic concept of the physical layer APS applied in the present invention.

FIG. 2 shows a configuration diagram of a node C and a node F located at either ends of a protection domain shown in FIG. 1.

FIG. 3 shows a configuration block diagram realizing a functional element of a demultiplexer (DMX) 3-2.

FIG. 4 shows a configuration block diagram of line interface portions 2'-1 to 2'-n in the downstream side of node C shown in FIG. 2.

FIG. 5 shows a configuration block diagram of line interface portions 2-1 to 2-n in the upstream side of node F shown in FIG. 2.

FIG. 6 shows an embodiment for setting an ACT bit into an ACT bit set table 25 promptly to reduce an APS switchover time.

FIG. 7 shows a configuration block diagram of a multiplexer (MUX) 3-1 shown in FIG. 2.

PREFERRED EMBODIMENTS OF THE INVENTION

An embodiment of the present invention is described hereinafter with the accompanied drawings wherein like numerals and symbols refer to like parts.

Prior to explaining the embodiments of the present invention, a basic concept of the 'physical layer APS' is explained first for easier understanding of the invention.

In FIG. 1, a general diagram of the physical layer APS is shown. A node terminating the ATM layer is shown indicating a

situation that a connection is currently established between a node A to a node B. ATM cells each consisting of a header and a payload are transmitted on the connection.

As routes of the connection, a path is being established through nodes C -D -E -F constituting a working channel, and also a path through nodes C -G -H -F constituting a protection channel. The duplicated channel segment consisting of the working channel and the protection channel is called a 'protected domain', to which the physical layer APS is applied.

Note that a transmission path shown in FIG. 1 does not mean a physical line, but the path means a virtual channel on the ATM layer.

In such a network configuration, the physical layer APS is a mechanism to switch over from a working channel to a protection channel in case a failure occurs at an arbitrary point on the working channel. The switchover is generally triggered by the detection of an alarm indicating signal on a virtual path and a virtual channel (VP/VC-AIS; hereafter simply referred to as AIS). The above AIS is detected at a terminating point (node F in the case of FIG. 1) of a segment which is defined as a protected domain of the connection.

For example, when a physical failure such as a breakdown of a fiber transmission line occurs between node C and node D, this situation is detected at node D, producing an AIS cell to forward from node D in the downstream direction (i.e. in the direction toward node F).

Here, the AIS cell is a cell containing an AIS in an ATM

cell header. The AIS cell is detected by node F at which the protected domain is terminated. On this detection, the relevant segment is declared inoperable. At the same time an APS procedure is started.

The APS can be classified into the following schemes with respect to the provision of protection channels. One method is that one protection channel is provided corresponding to each working channel i.e. 1+1 or 1:1 scheme; the other is, using a shared protection channel, either one protection channel shared by n working channels i.e. 1:n scheme, or m protection channels shared by n working channels i.e. m:n scheme ($m \leqq n$).

The difference between 1+1 scheme and 1:1 scheme is that in 1+1 scheme the identical cells are normally transmitted on both a working channel and a protection channel, while in 1:1 scheme cells are transmitted only on a channel currently in working state (i.e. a working channel).

From another aspect, the APS can be classified into a VP/VC-APS method in which a switchover is carried out at the unit of each VP/VC (virtual path and virtual channel) connection, and a VPG/VCG-APS method in which a switchover is carried out at the unit of a group of VP/VC connections.

The object of the present invention is to realize the above-mentioned physical layer APS with a simplified configuration.

In FIG. 2, there is shown a configuration example of a node in accordance with the present invention. The node is located at either end of a protection domain shown in FIG. 1. Only node C and node F are shown in this figure where other intermediate

nodes are omitted.

Each node consists of an ATM switching system which is provided with the following elements: an ATM switch circuit (SW) 1 for performing cell switching function; line interface portions (LINF) 2'-1 to 2'-n for inserting cells, located at the external line side; and line interface portions (LINF) 2-1 to 2-n for extracting cells, located at the internal line side.

Also, there are provided in each node a multiplexer (MUX) 3-1 for multiplexing cells input from line interface portions 2-1 to 2-n, interfacing ATM switch circuit 1; a demultiplexer (DMX) 3-2 for demultiplexing multiplexed ATM cells, also interfacing ATM switch circuit 1; and a controller 4 for performing overall control function.

Referring to FIG. 2, an operation of the physical layer APS in accordance with the present invention is explained hereafter, where 1+1 or 1:1 scheme is taken as an example.

(1) At an initial state, the identical cells are being transmitted on both working channels and protection channels. In node C, a connection for the APS is identified at demultiplexer (DMX) 3-2 under the control of controller 4, to duplicate cells on a working channel side to a protection channel side.

(2) When a failure occurs on a working channel between node C and node D, node D detects the failure and then transmits an AIS cell in the downstream direction toward node F. This AIS cell is detected by node F, of which information is transferred to controller 4.

(3) Controller 4 orders to switch over the connection (ACT) for the APS. Specifically, controller 4 orders ATM switch circuit 1 to switch over from line interface portion (LINF) 2-1 where the working channel is terminated to line interface portion (LINF) 2-i where the protection channel is terminated. More specifically, using a function provided in each line interface portion (LINF) 2-1 to 2-n, an ACT bit in each ATM cell header in transmission is set either 'ON' (which denotes line interface portion 2-i i.e. the protection channel side is in working state), or 'OFF' (which denotes line interface portion 2-1 i.e. the working channel side is in working state).

(4) A mechanism is provided in multiplexer (MUX) 3-1 that the ACT bit in each cell received from line interface portions 2-1 to 2-n is examined to determine whether the cell is to be transmitted. Only cells having proper ACT indication are allowed to transmit. In multiplexer (MUX) 3-1 in node F, a previous condition that only ATM cells received on the working channel are transmitted through and ATM cells on the protection channel are rejected to transmit, is now switched over to that only ATM cells received on the protection channel can be transmitted through. Thus an operation of the physical layer APS is completed.

According to the present invention, the following functional elements are provided for realizing a sequence of operation described above in an ATM node;

(1) in demultiplexer (DMX) 3-2, duplicating cells on a working channel to a protection channel side at the unit of

either a connection or a connection group,

(2) in line interface portions 2-1 to 2-n, providing each ATM cell header with an ACT bit for specifying ACT (in working condition) at the unit of either a connection or a connection group, and

(3) in multiplexer (MUX) 3-1, transmitting only cells of which ACT is specified in each cell header.

A detailed embodiment of the functional elements (1) to (3) above is described hereinafter.

In FIG. 3, a functional element of demultiplexer (DMX) 3-2 provided in each node is shown.

In this FIG. 3, Tag-B is a tag provided in an ATM cell header for identifying an output channel. O-ICID-A is also provided in the ATM cell header, which is an 'internal channel identifier' for identifying a channel in an output channel indicated by Tag-B.

An APS identifier is also provided in the ATM cell header which enables to determine whether a connection (or a connection group) of the relevant cell is object for the APS processing or not.

The tag and the internal channel identifier explained above are set into an ATM cell header at either line interface portions 2-1 to 2-n and 2'-1 to 2'-n, multiplexer (MUX) 3-1, or ATM switch circuit 1, under the control of controller 4.

For example, in node C shown in FIG. 3, an APS identifier in an ATM cell input to demultiplexer (DMX) 3-2 is examined. If this APS identifier indicates the cell is object for the APS

(i.e. APS is 'ON'), then a cell duplication table 30 is referred to, using Tag-B and O-ICID-A as the reference keys.

Through the above procedure, information on an output line Tag-B(P) to be used for an protection channel and a channel O-ICID-A(P) in the above output line is obtained. Then the ATM cell is duplicated and the information on an output line and a channel in the duplicated cell are respectively replaced by Tag-B(P) and O-ICID-A(P), to output to a cell buffer (FIFO) 31.

INS A10

A10 In FIG. 4, there is illustrated a configuration block diagram of line interface portion 2-i on the internal line side which is provided in node D, for example, located in the downstream direction against node C. In this FIG. 4, O-VPI/VCI is stored in a cell header, showing a value of VPI/VCI (virtual path and virtual channel identifier) of an output line related to the cell.

INS A11

A11 Using as a reference key an internal line and channel identifier O-ICID-A in an input ATM cell, a VPI/VCI conversion table 21 is referred to. Then, VPI/VCI to be forwarded to an external line is obtained from VPI/VCI conversion table 21.

The obtained VPI/VCI is set into the ATM cell header in a header modification portion 22, to forward to the external transmission line.

INS A12

A12 Also, in line interface portion 2-i on the internal line side, there is provided an alarm cell insertion circuit 20 to insert an alarm cell named VP/VC-AIS. When a failure occurs between node C and node D, and node D detects this failure, an alarm cell is inserted according to a control command issued

from controller 4.

Here, an alarm cell is a kind of ATM cell in which an alarm indicating signal (AIS) is set in an ATM cell header. The alarm cell is detected in the downstream node (for example, node F in the network configuration shown in Fig. 1) to trigger THE APS operation.

In FIG. 5, there is shown a block diagram of a configuration example related to the input side of line interface portion 2-1 in node F which constitutes a terminal node of a protected domain. By referring to an ICID conversion table 23 using VPI/VCI, which is an external virtual path and virtual channel identifier stored in a header of an input ATM cell, as a reference key, a corresponding internal virtual path and virtual channel identifier, I-ICID-A, is obtained.

The reason of the above processing is that VPI/VCI composed of 22 bits requires large amount of circuits to process in ATM switch circuit 1. Therefore, VPI/VCI is converted into I-ICID-A which is a condensed form of the internal path and channel identifier. A header modification portion 24 replaces with the obtained I-ICID-A in an ATM cell header which.

Then, using the obtained I-ICID-A as a reference key, an APS identifier set table 25 is referred to. Depending on 'ON' or 'OFF' of an APS bit in APS identifier set table 25, whether the corresponding internal path and channel is object for the APS or not is determined.

Furthermore, using the value of I-ICID-A as a reference key, an ACT bit set table 26 is referred to. The ACT bit indicates

whether each object cell for the APS is actually to be transmitted to a destination terminal.

The APS bit and the ACT bit which have been referred to are attached to an ATM cell header by a header modification portion 27.

INS A16

Values in those tables for determining that a cell is object for the APS etc. are set by an order from controller 4 either in advance or in case necessary.

Furthermore, in FIG. 5, an alarm cell extraction portion 28 is provided for extracting an alarm cell sent from an upstream node to inform to controller 4.

INS A15

In FIG. 6, there is shown an embodiment for setting APS identifier set table 25 and ACT bit set table 26 by an order from controller 4 which is carried out in a procedure after the APS is started. The embodiment intends to shorten the required time for an APS switchover by setting ACT bit set table 25 with high-speed.

INS A17

In FIG. 5, when an APS switchover occurs, it is necessary to rewrite all data related to the corresponding connection in ACT bit set table 25, which may necessitate large processing time.

INS A18

On the other hand, according to the configuration shown in FIG. 6, a table 25 is provided for use of setting ACT bits at the unit of an APS group (APS-Gr.). This enables to set the table from controller 4 at the unit of APS group i.e. in a batch of lines, instead of individual line by line, with less processing time.

INS A19

A19 In order to refer to this table 25, information is required to identify which APS group each connection belongs to. For this purpose, an APS group conversion table 29 is provided for obtaining APS-Gr from I-ICID-A having been extracted from ICID conversion table 23. Each APS group is generally assigned corresponding to each outgoing line of ATM switch circuit 1.

INS A20

A20 Using an APS group obtained from APS group conversion table 29, an APS identifier set table 26 is referred to. Also ACT bit set table 25 is referred to using an APS group obtained from APS group conversion table 29.

In FIG. 7, there is shown a configuration block diagram of multiplexer (MUX) 3-1 shown in FIG. 2. Among ATM cells received from each channel route SHW0 to SHWn, only ATM cells received on a protection channel side having 'ON' in each ACT bit are transmitted through cell invalidation circuits 32-1 to 32-n. ATM cells transmitted through are then multiplexed by a multiplexing circuit 33 to forward to ATM switch circuit 1.

Having been explained referring to the accompanied drawings, the present invention provides a concrete configuration for realizing ATM layer protection switching (APS). An ATM switching system according to the present invention can be provided with simple configuration.

The foregoing description of the embodiment is not intended to limit the invention to the particular examples. Any suitable modification may be resorted to the scope of the invention. All features and advantages of the invention which fall within the scope of the invention are covered by the appended claims.